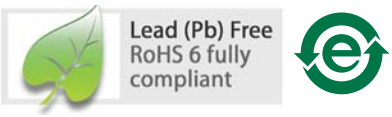
ADNS-9500

LaserStream™ Gaming Sensor

Data Sheet



Description

The ADNS-9500 LaserStream gaming sensor comprises of sensor and VCSEL in a single chip-on-board (COB) package. ADNS-9500 provides enhanced features like programmable frame rate, programmable resolution, configurable sleep and wake up time to suit various PC gamers' preferences.

The advanced class of VCSEL was engineered by Avago Technologies to provide a laser diode with a single longitudinal and a single transverse mode.

This LaserStream gaming sensor is in 16-pin integrated chip-on-board (COB) package. It is designed to be used with ADNS-6190-002 small form factor (SFF) gaming laser lens to achieve the optimum performance featured in this document. These parts provide a complete and compact navigation system without moving part and laser calibration process is NOT required in the complete mouse form, thus facilitating high volume assembly.

Theory of Operation

The sensor is based on LaserStream technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement. It contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a four wire serial port. The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the Δx and Δy relative displacement values. An external microcontroller reads the Δx and Δy information from the sensor serial port. The microcontroller then translates the data into PS2, USB, or RF signals before sending them to the host PC or game console.

Features

- Small form factor chip-on-board package
- Dual power supply selections, 3V or 5V
- VDDIO range: 1.65 – 3.3V
- 16-bits motion data registers
- High speed motion detection at 150ips and acceleration up to 30g
- Advanced technology 832-865nm wavelength VCSEL
- Single mode lasing
- No laser power calibration needed
- Compliance to IEC/EN 60825-1 Eye Safety
  - Class 1 laser power output level
  - On-chip laser fault detect circuitry
- Self-adjusting frame rate for optimum performance
- Motion detect pin output
- Internal oscillator – no external clock input needed
- Enhanced Programmability
  - Frame rate up to 11,750 fps
  - 1 to 5 mm lift detection
  - Resolution up to 5000cpi with ~90cpi step
  - X and Y axes independent resolution setting
  - Register enabled Rest Modes
  - Sleep and wake up times

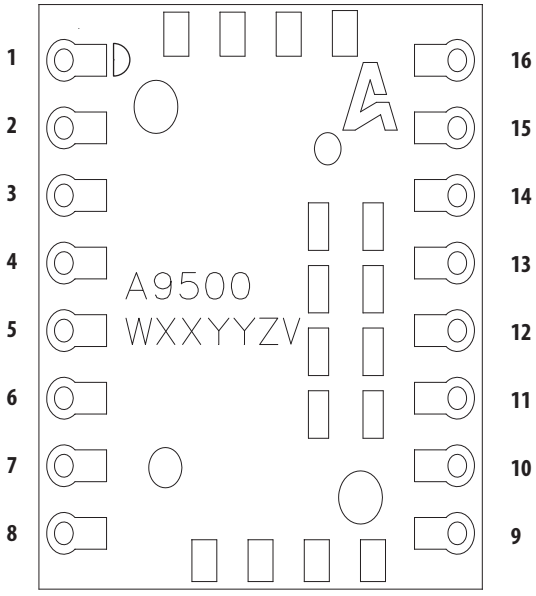
Applications

- Corded and cordless gaming laser mice
- Optical trackballs
- Motion input devices

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Pinout of ADNS-9500 Optical Mouse Sensor

Pin No	Pin Name for 5V mode	Pin Name for 3V mode	Description
1	+VCSEL	+VCSEL	Positive Terminal Of VCSEL
2	LASER_NEN	LASER_NEN	LASER Enable (Active Low Output)
3	NCS	NCS	Chip Select (Active Low Input)
4	MISO	MISO	Serial Data Output (Master In/Slave Out)
5	SCLK	SCLK	Serial Clock Input
6	MOSI	MOSI	Serial Data Input (Master Out/Slave In)
7	MOTION	MOTION	Motion Detect (Active Low Output)
8	XYLASER	XYLASER	Laser Current Output Control
9	VDD5	VDD3	5V input for 5V mode 3V Input for 3V mode
10	PWR_OPT (GND)	PWR_OPT (VDD3)	Power Option: Connect to GND for 5V Mode Connect to VDD3 for 3V Mode
11	GND	GND	Analog Ground
12	REFB	VDD3	3V Regulator Output for 5V Mode 3V Input for 3V Mode
13	REFA	REFA	1.8V Regulator Output
14	DGND	DGND	Digital Ground
15	VDDIO	VDDIO	IO Voltage Input (1.65 - 3.3V)
16	-VCSEL	-VCSEL	Negative Terminal Of VCSEL



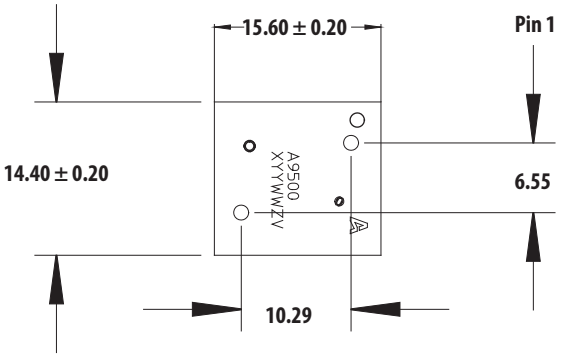
W = Subcon Code

XXYY = Date Code

Z = Sensor Die Source

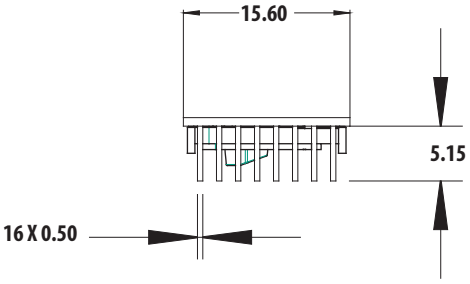
V = VCSEL Die Source

Figure 1. Package Pinout

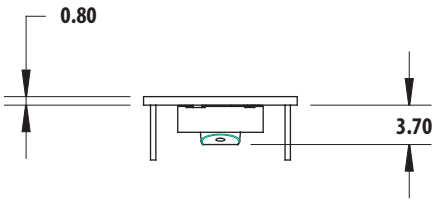


TOP VIEW

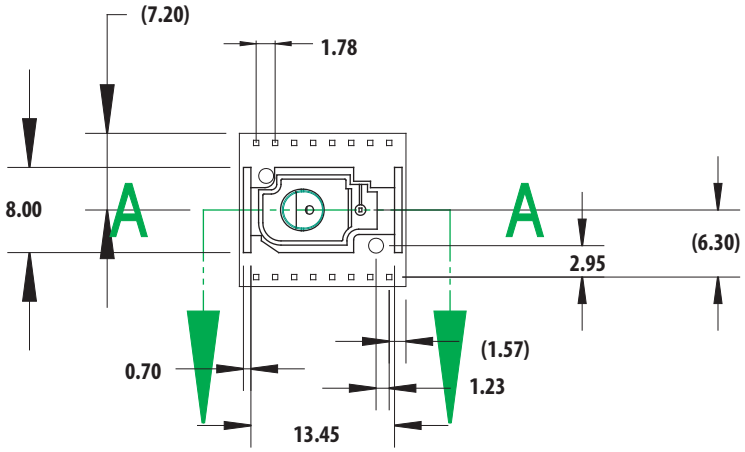
Notes:
1. Dimensions in millimeter
2. Dimension tolerance ±0.1mm unless specified otherwise
3. Coplanarity of leads: 0.15mm
4. Lead pitch tolerance: ±0.15mm
5. Non-cumulative lead pitch tolerance ±0.15mm
6. Maximum flash +0.2mm
7. Lead width: 0.5mm
8. Bracket ( ) indicates reference dimensions



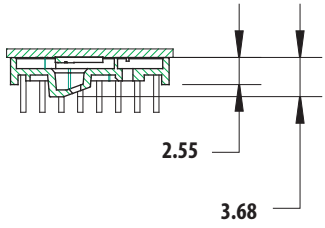
FRONT VIEW



RIGHT VIEW



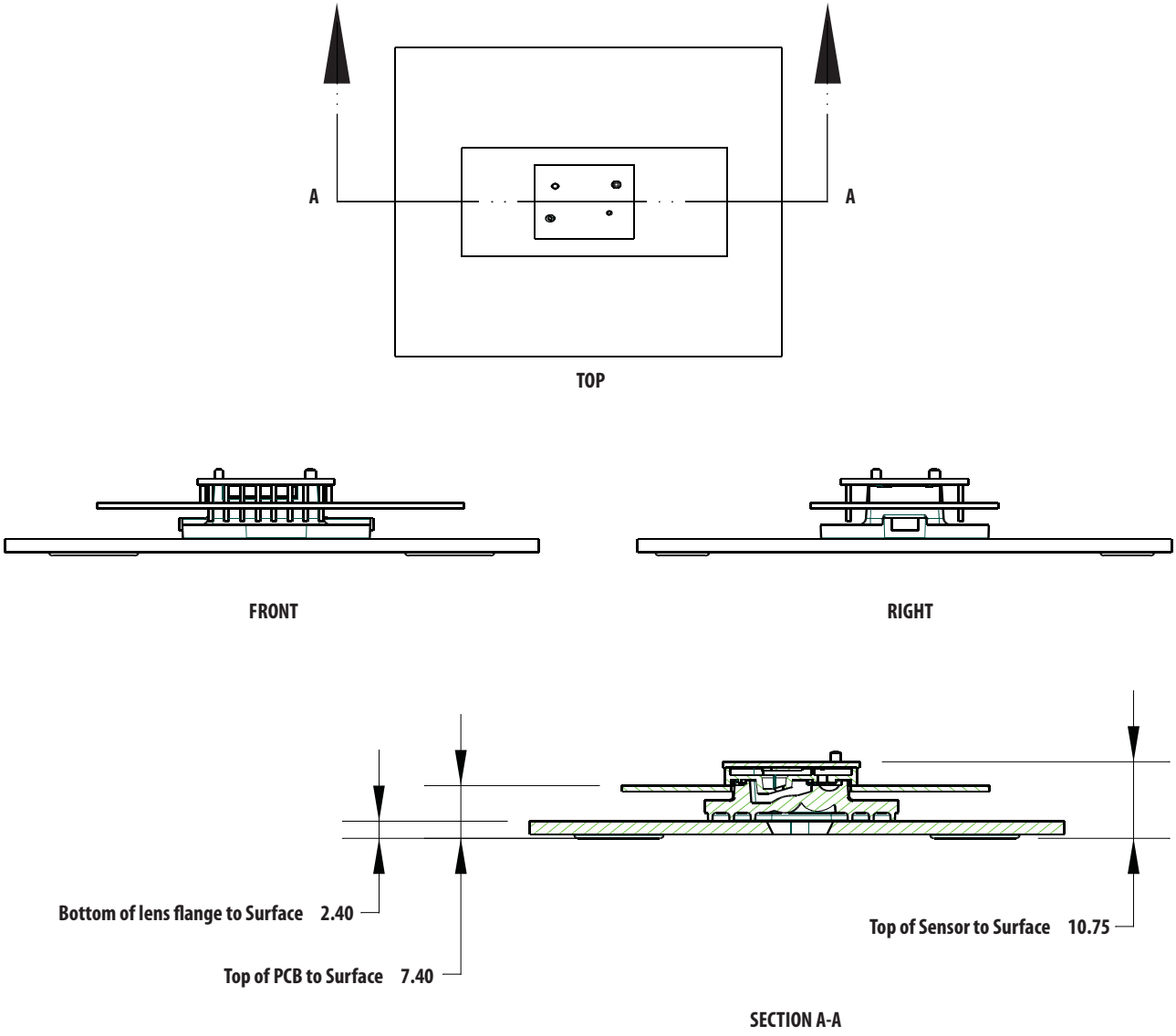
BOTTOM VIEW



SECTION A - A

Figure 2. Package outline drawing

Overview of Laser Mouse Sensor Assembly



Note: Dimensions in millimeter and for reference only

Figure 3. 2D Assembly drawing of ADNS-9500 sensor and ADNS-6190-002 lens coupled with PCB and base plate

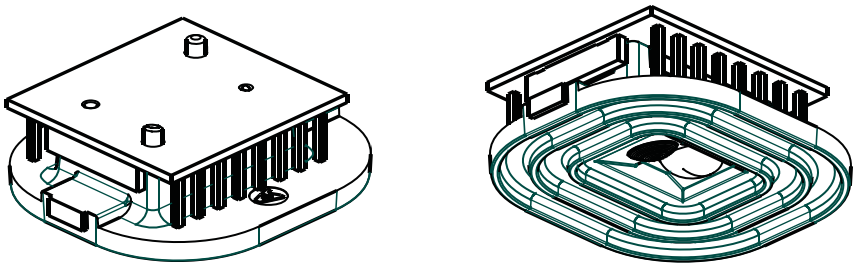


Figure 4. Isometric drawing of ADNS-9500 sensor and ADNS-6190-002 lens

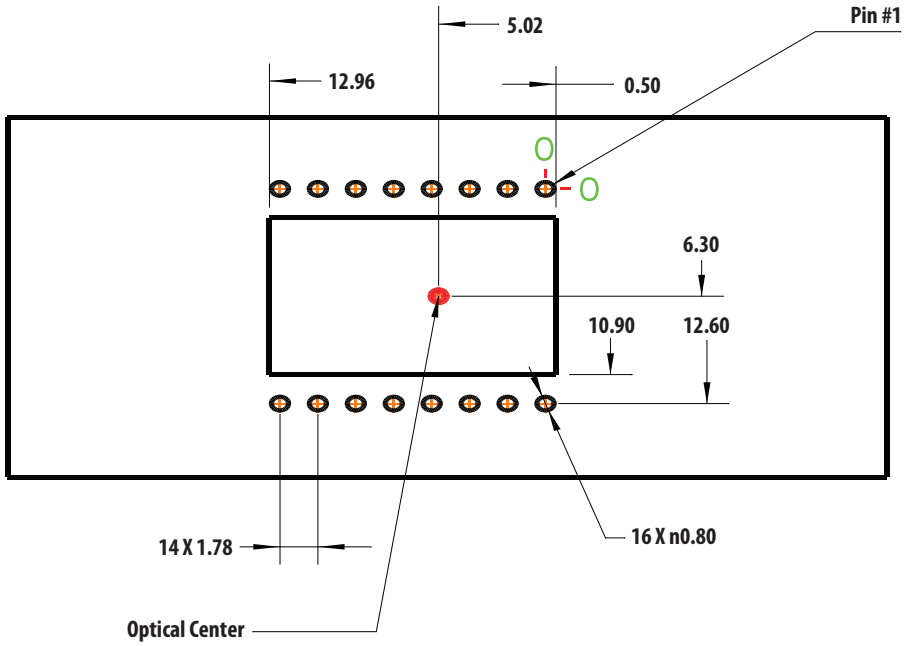


Figure 5. Recommended PCB mechanical cutouts and spacing

Assembly Recommendation

1. Insert the COB sensor and all other electrical components into the application PCB.
2. Wave-solder the entire assembly in a no-wash soldering process utilizing a solder fixture. The solder fixture is needed to protect the sensor during the solder process. The fixture should be designed to expose the sensor leads to solder while shielding the optical aperture from direct solder contact.
3. Place the lens onto the base plate. Care must be taken to avoid contamination on the optical surfaces.
4. Remove the protective kapton tapes from the optical aperture of the sensor and VCSEL respectively. Care must be taken to keep contaminants from entering the aperture.
5. Insert the PCB assembly over the lens onto the base plate. The sensor package should self-align to the lens. The optical position reference for the PCB is set by the base plate and lens. The alignment guide post of the lens locks the lens and integrated molded lead-frame DIP sensor together. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
6. Optional: The lens can be permanently locked to the sensor package by melting the lens' guide posts over the sensor with heat staking process.
7. Install the mouse top case. There must be a feature in the top case (or other area) to press down onto the sensor to ensure the sensor and lenses are interlocked to the correct vertical height.

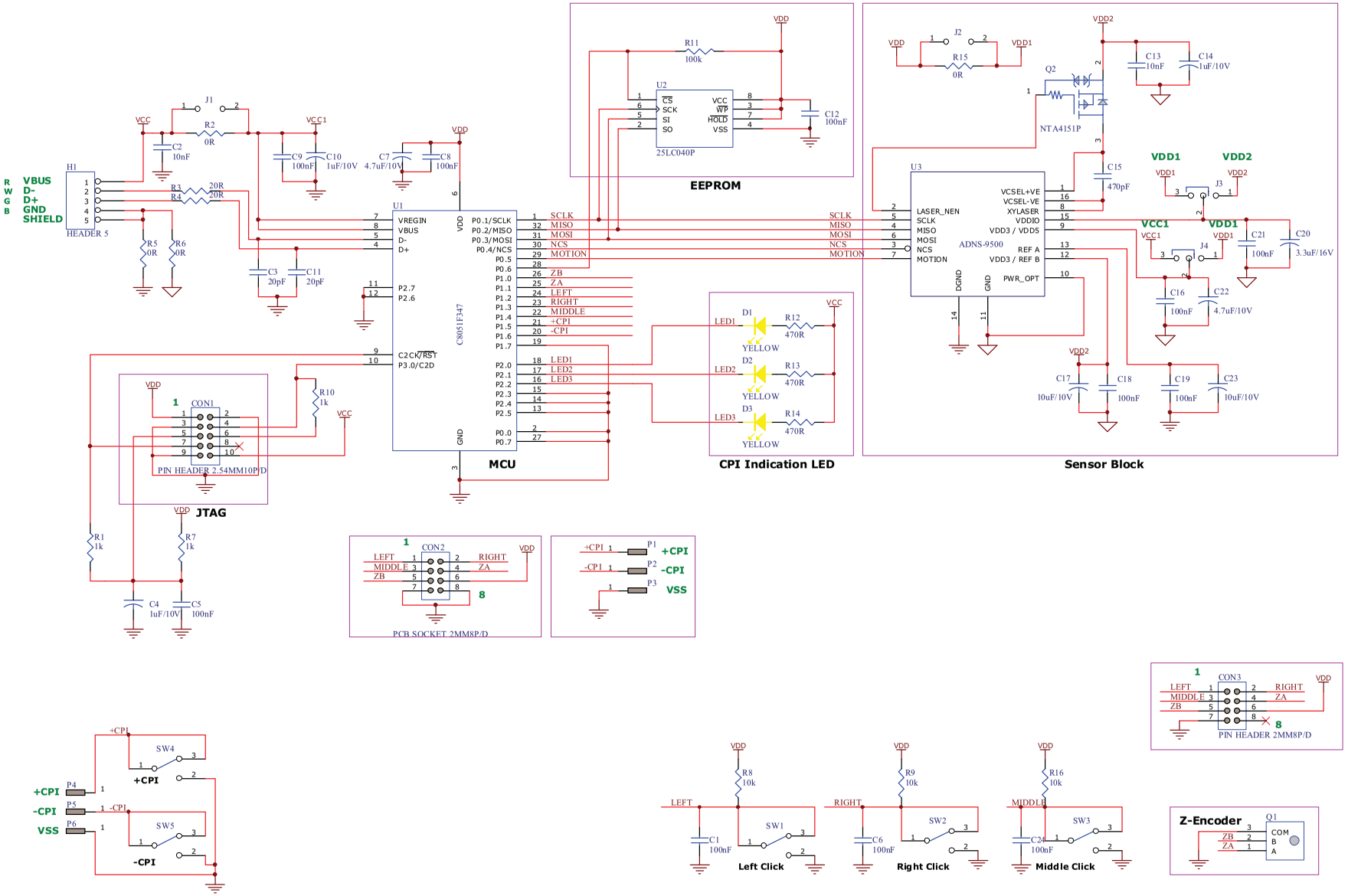


Figure 6a. Schematic Diagram for 5V Corded Mouse

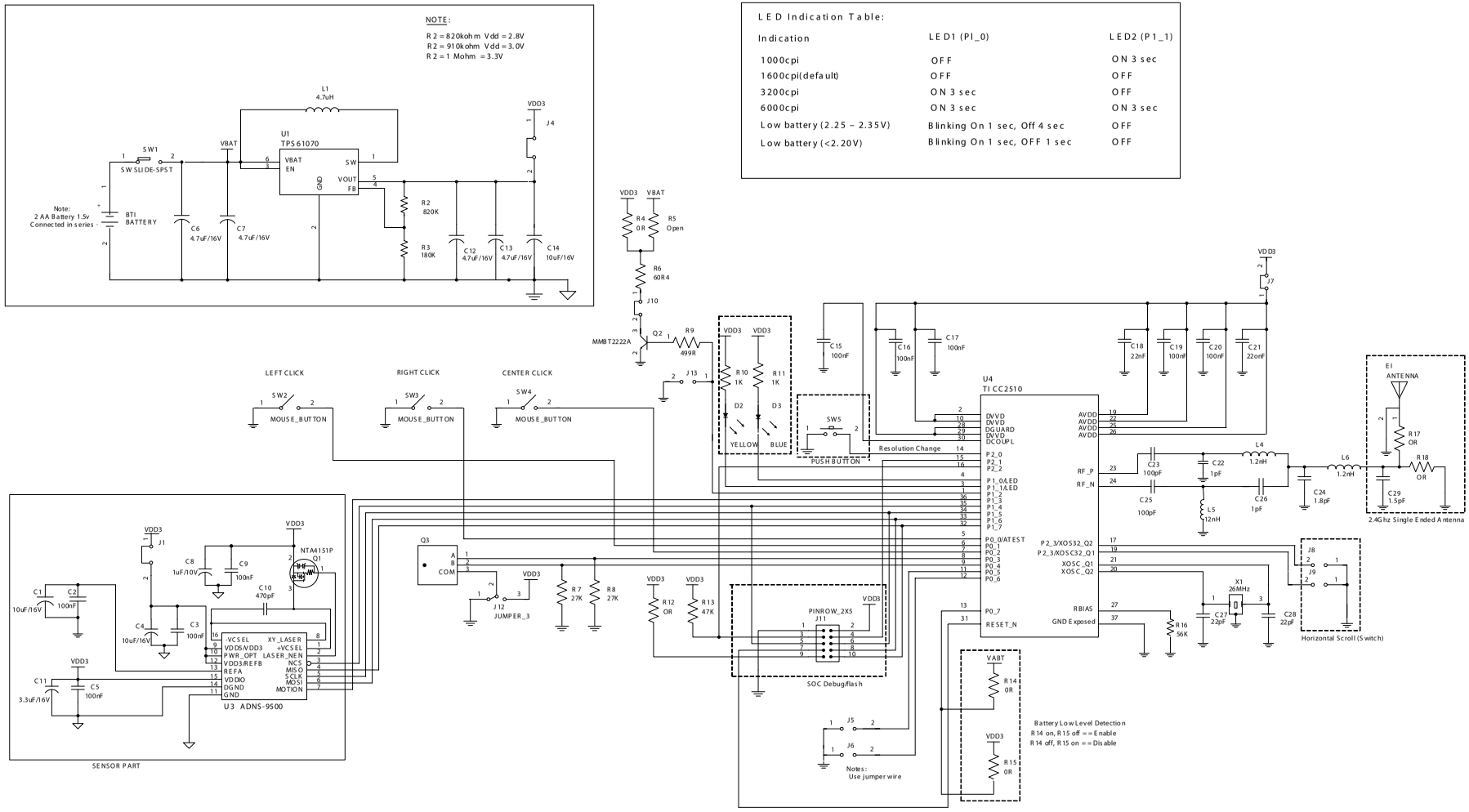


Figure 6b. Schematic Diagram for 3V Cordless Mouse

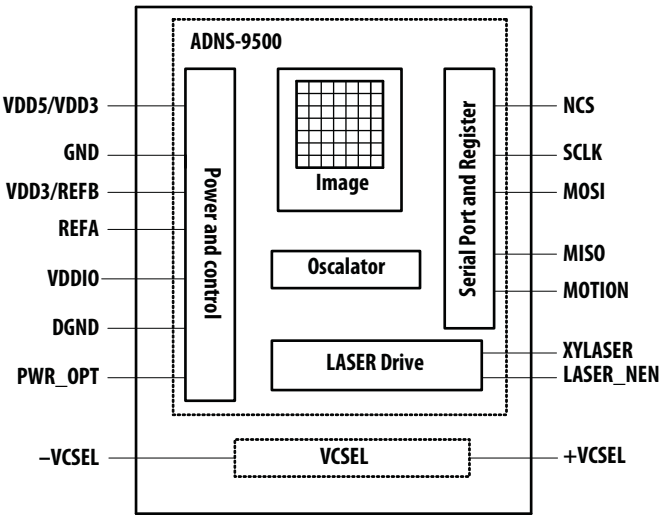


Figure 7. Block diagram of ADNS-9500

Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled into a mouse with shielded cable and following Avago recommendations.
- Passes IEC-1000-4-3 radiated susceptibility level when assembled into a mouse with shielded cable and following Avago recommendations.
- Passes EN61000-4-4/IEC801-4 EFT tests when assembled into a mouse with shielded cable and following Avago recommendations.
- Passes IEC-61000-4-2 Electrostatic Discharge Immunity Test (ESD) and provides sufficient ESD creepage/ clearance distance to withstand discharge up to 15KV when assembled into a mouse according to usage instructions above.
- Passes IEC/EN 60825-1 Eye Safety Class 1 when operating with the laser output power pre-calibrated by Avago Technologies without external hardware and software control of laser current.

Design Considerations for Improving ESD Performance

For improved electrostatic discharge performance, typical creepage and clearance distance are shown in the table below. Assumption: base plate construction as per the Avago supplied 3D model file when use with ADNS-6190-002 lens. The lens flange can be sealed (i.e. glued) to the base plate. Note that the lens material is polycarbonate and therefore, cyanoacrylate based adhesives or other adhesives that may damage the lens should NOT be used.

Typical Distance (mm)	ADNS-6190-002
Creepage	17.3
Clearance	1.8

Eye Safety

The ADNS-9500 sensor and the associated components in the schematic of Figure 6 are intended to comply with Class 1 Eye Safety Requirements of IEC 60825-1. Avago Technologies calibrates the sensor's laser output power (LOP) to Class 1 eye safety level and store the registers values that control the LOP prior shipping out, thus no LOP calibration is required in complete mouse system at manufacturer site.

ADNS-9500 sensor is designed to maintain the laser output power using ADNS-6190-002 lens within Class 1 Eye Safety requirements over components manufacturing tolerances under the recommended operating conditions and application circuits of Figure 6 as specified in this document. Under normal operating conditions, the sensor generates the drive current for the VCSEL. Increasing the LOP by other means on hardware and software can result in a violation of the Class 1 eye safety limit of 716μW. For more information, please refer to Eye Safety Application Note.

LASER Drive Mode

The laser is driven in pulsed mode during normal operation. A calibration mode is provided which drives the laser in continuous (CW) operation for testing purpose.

The default setting of laser is in Forced_Disable mode, which the laser is turned OFF. The laser have to be turned ON during power up sequence by setting Forced_ Disabled bit (Bit-0) of LASER_CTRL0 register to 0.

Disabling the LASER

LASER_NEN is connected to the gate of an external P-channel MOSFET transistor which, when ON connects REFB to the laser. In normal operation, LASER_NEN is low. In the case of a fault condition, LASER_NEN goes high to turn the transistor off and disconnect REFB from the laser.

LASER Output Power (LOP)

The LOP can be measured for testing purpose as per steps below.

1. Power up reset the mouse system.
2. Enable the laser by setting Forced_Disabled bit of LASER_CTRL0 register (address 0x20) to 0.
3. Enable the Calibration mode by writing 010b to bits [3,2,1] of LASER_CTRL0 register (address 0x20) to set the laser to continuous (CW) mode.
4. Measure the LOP at the navigation surface plane.

The pre-calibrated LOP value at typical operating supply voltage and temperature of 25 ± 5°C should not exceeding 506µW, otherwise the LOPmax limit in the Absolute Maximum Rating is applicable. The following conditions apply:

- The system is operated within the recommended operating supply voltage and temperature range.
- In 3V mode, the VDD3 value is no greater than 300mV above the pre-calibration voltage of 3.0V. In 5V mode, REFB should be used to drive the PMOSFET connecting to VCSEL.
- No allowance for optical power meter accuracy is assumed.

Single Fault Detection

ADNS-9500 sensor is able to detect a short circuit or fault condition at –VCSEL pin, which could lead to excessive laser output power. A leakage path to ground on this node will trigger the fault detection circuit, which will turn off the laser drive current source and set the LASER_NEN output high. When used in combination with external component as shown in the block diagram below, the system will prevent excessive laser power for a resistive path at XY_LASER by shutting off the laser. In addition to the ground path fault detection described above, the fault detection circuit is periodically checking for proper operation by internally generating a path to ground with the laser turned off via LASER_NEN. If the –VCSEL pin is shorted to VDD5, VDD3, REFA or REFB pin, this test will fail and will be reported as a fault.

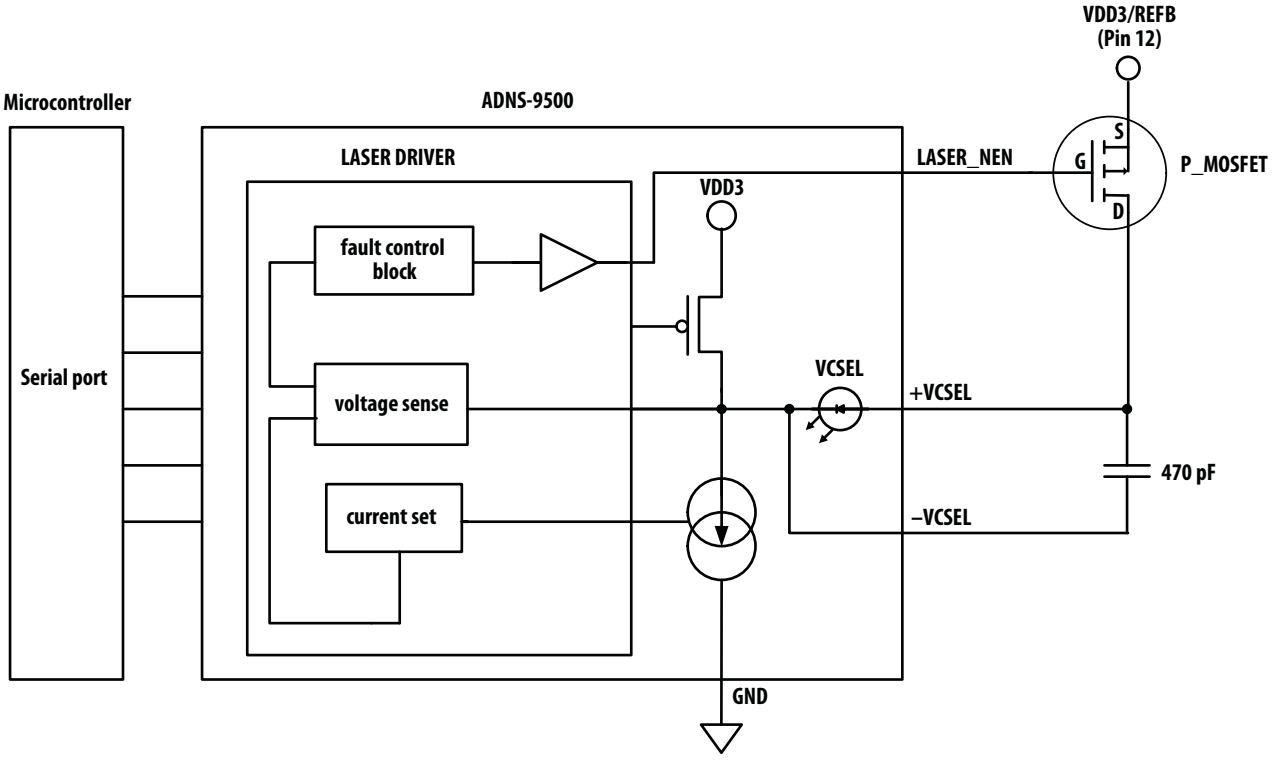


Figure 8. Single Fault Detection and Eye-safety Feature Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Lead-Free Solder Temp			260	°C	For 7 seconds, 1.8mm below seating plane. Refer to soldering reflow profile in PCB Assembly & Soldering Considerations Application Note AN 5023.
Supply Voltage	V_{DD5}	-0.5	5.5	V	
	V_{DD3}	-0.5	3.4	V	
	V_{DDIO}	-0.5	3.4	V	
ESD (Human body model)			2	kV	All Pins
Input Voltage	V_{IN}	-0.5	3.4	V	All I/O Pins
Laser Output Power	LOP_{max}		716	µW	Class 1 Eye Safety Limit

Comments:

1. *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are the stress ratings only and functional operation of the device at these or any other condition beyond those indicated for extended period of time may affect device reliability.*
2. *The inherent design of this component causes it to be sensitive to electrostatic discharge. The ESD threshold is listed above. To prevent ESD-induced damage, take adequate ESD precautions when handling this product.*

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Operating Temperature	T_A	0		40	°C	
Supply voltage	V_{DD5}	4.0	5.0	5.25	Volts	Including Supply Noise for 5V mode
	V_{DD3}	2.7	2.8	3.3	Volts	Including Supply Noise for 3V mode
	V_{DDIO}	1.65		3.3	Volts	Including noise.
Power supply rise time	V_{RT5}	1		100	ms	0 to 5.0V for 5V mode
	V_{RT3}	1		100	ms	0 to 2.8V for 3V mode
Supply noise (Sinusoidal)	V_{NA}			100	mV_{p-p}	50kHz - 50MHz
Serial Port Clock Frequency	f_{SCLK}			2	MHz	Active drive, 50% duty cycle
Distance from lens reference plane to surface	Z	2.18	2.40	2.62	mm	Results in +/- 0.22mm minimum DOF. Refer to Figure 9.
Speed	S		150	200	ips	inch/sec Maximum speed performance on select gaming surfaces.
Acceleration	A			30	g	In Run mode only
Load Capacitance	C_{out}			100	pF	MOTION, MISO
Frame Rate	FR			11,750	fps	Frame per second
VCSEL Peak Wavelength	λ	832		865	nm	

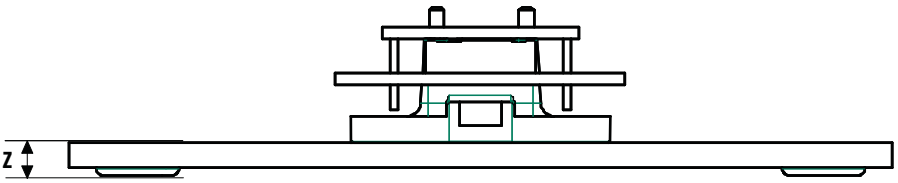


Figure 9. Distance from lens reference plane to surface, Z

AC Electrical Specifications

Electrical Characteristics over recommended operating conditions. (Typical values at 25 °C, VDD3 = 2.8V, VDDIO = 1.8V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Motion delay after reset	$t_{MOT-RST}$	30			ms	From SW_RESET register write to valid motion, assuming motion is present
Shutdown	t_{STDWN}			500	ms	From Shutdown mode active to low current
Wake from shutdown	t_{WAKEUP}	30			ms	From Shutdown mode inactive to valid motion. Notes: A RESET must be asserted after a shutdown. Refer to Shutdown section, also note $t_{MOT-RST}$
Forced Rest enable	$t_{REST-EN}$			1	s	From RESTEN bits set to low current
Wake from Forced Rest	$t_{REST-DIS}$			1	s	From RESTEN bits cleared to valid motion
MISO rise time	t_{r-MISO}		50	200	ns	C_L = 100pF
MISO fall time	t_{f-MISO}		50	200	ns	C_L = 100pF
MISO delay after SCLK	$t_{DLY-MISO}$			120	ns	From SCLK falling edge to MISO data valid, no load conditions
MISO hold time	$t_{hold-MISO}$	200			ns	Data held until next falling SCLK edge
MOSI hold time	$t_{hold-MOSI}$	200			ns	Amount of time data is valid after SCLK rising edge
MOSI setup time	$t_{setup-MOSI}$	120			ns	From data valid to SCLK rising edge
SPI time between write commands	t_{SWW}	120			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI time between write and read commands	t_{SWR}	120			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte.
SPI time between read and subsequent commands	t_{SRW} t_{SRR}	20			µs	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command.
SPI read address-data delay	t_{SRAD}	100			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read.
NCS inactive after motion burst	t_{BEXIT}	500			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS to SCLK active	$t_{NCS-SCLK}$	120			ns	From last NCS falling edge to first SCLK rising edge
SCLK to NCS inactive (for read operation)	$t_{SCLK-NCS}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer
SCLK to NCS inactive (for write operation)	$t_{SCLK-NCS}$	20			us	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer
NCS to MISO high-Z	$t_{NCS-MISO}$			500	ns	From NCS rising edge to MISO high-Z state
MOTION rise time	$t_{r-MOTION}$		50	200	ns	C_L = 100pF
MOTION fall time	$t_{f-MOTION}$		50	200	ns	C_L = 100pF
Transient Supply Current	I_{DDT5}			90	mA	Max supply current during a V_{DD5} ramps from 0 to 5.0V
	I_{DDT3}			65	mA	Max supply current during a V_{DD3} ramps from 0 to 2.8V

DC Electrical Specifications

Electrical Characteristics over recommended operating conditions.

For 3V mode, Typical values at 25°C, V_{DD} = 2.8 V, V_{DDIO} = 2.8V. For 5V mode, Typical values at 25°C, V_{DD} = 5.0 V, V_{DDIO} = REFB

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
DC Supply Current in 3V mode	I_{DD_RUN3}		33	45	mA	Average current, including LASER current. No load on MISO, MOTION.
	I_{DD_REST1}		0.26	0.4	mA	
	I_{DD_REST2}		0.12	0.2	mA	
	I_{DD_REST3}		0.08	0.15	mA	
DC Supply Current in 5V mode	I_{DD_RUN5}		36	50	mA	
Peak Supply Current	I_{DDP3}			60	mA	For 3V mode
	I_{DDP5}			65	mA	For 5V mode
Shutdown Supply Current	$I_{DDSTDWN}$		65	140	µA	NCS, SCLK, MOSI = VDDIO MISO = GND
REFB Output Voltage	V_{REFB}	2.85	3.05	3.25	V	Do not connect this pin as a supply to other chips other than the integrated VCSEL and VDDIO
Input Low Voltage	V_{IL}			$0.3*V_{DDIO}$	V	SCLK, MOSI, NCS
Input High Voltage	V_{IH}	$0.7*V_{DDIO}$			V	SCLK, MOSI, NCS
Input Hysteresis	V_{I_HYS}		100		mV	SCLK, MOSI, NCS
Input Leakage Current	I_{leak}		±1	±10	µA	Vin = 0.7*VDDIO , SCLK, MOSI, NCS
Output Low Voltage, MISO, MOTION	V_{OL}			$0.3*V_{DDIO}$	V	Iout = 1mA, MISO, MOTION
Output High Voltage, MISO, MOTION	V_{OH}	$0.7*V_{DDIO}$			V	Iout = -1mA, MISO, MOTION
Output Low Voltage, LASER_NEN	V_{OL}			$0.3*V_{REFB}$	V	Iout = 1mA, LASER_NEN
Output High Voltage, LASER_NEN	V_{OH}	$0.7*V_{REFB}$			V	Iout = -0.5mA, LASER_NEN
Input Capacitance	C_{in}			10	pF	MOSI, NCS, SCLK

Sensor's Typical Performance Characteristics

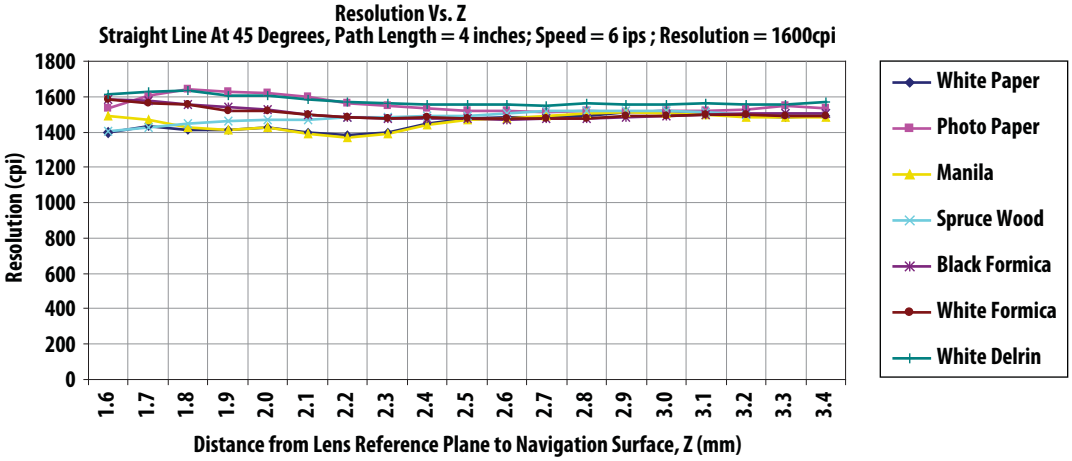


Figure 10. Mean Resolution vs. Z at default resolution at 1600cpi

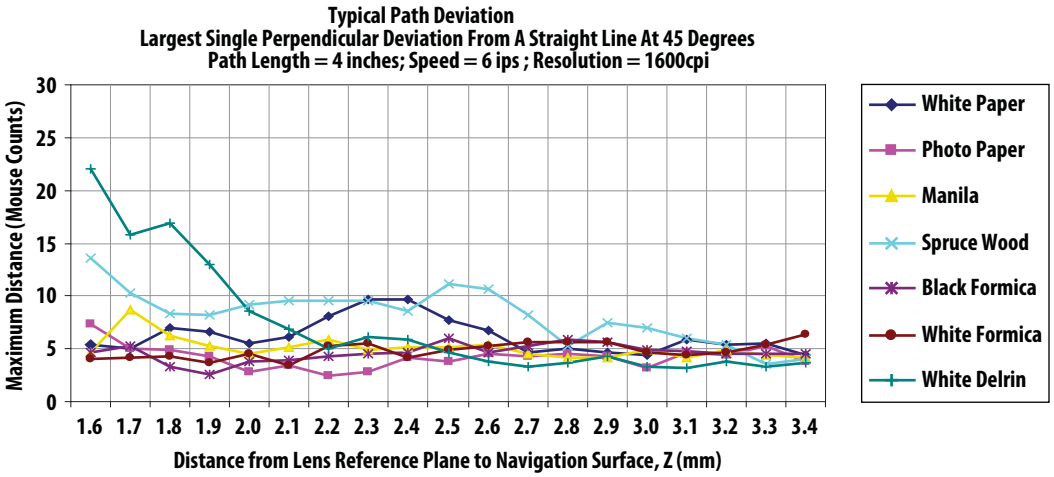


Figure 11. Average Error vs. Distance at default resolution at 1600cpi (mm)

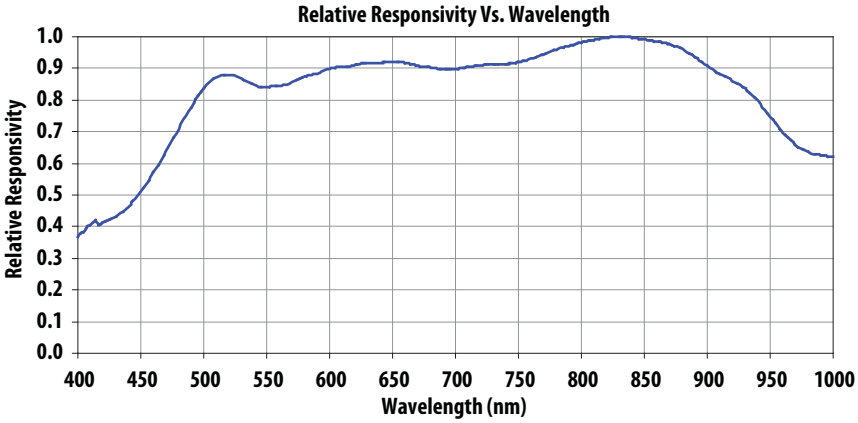


Figure 12. Wavelength Responsivity

Synchronous Serial Port

The synchronous serial port is used to set and read parameters in the ADNS-9500 Sensor, and to read out the motion information. The serial port is also used to load PROM data into the ADNS-9500 Sensor.

The port is a four wire port. The host micro-controller always initiates communication; the ADNS-9500 Sensor never initiates data transfers. SCLK, MOSI, and NCS may be driven directly by a micro-controller. The port pins may be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored and the output is tri-stated.

The lines that comprise the SPI port are:

SCLK: Clock input. It is always generated by the master (the micro-controller).

MOSI: Input data. (Master Out/Slave In)

MISO: Output data. (Master In/Slave Out)

NCS: Chip select input (active low). **NCS** needs to be low to activate the serial port; otherwise, **MISO** will be high Z, and **MOSI** & **SCLK** will be ignored. **NCS** can also be used to reset the serial port in case of an error.

Motion Pin

The motion pin is an active low output that signals the micro-controller when motion has occurred. The motion pin is lowered whenever the motion bit is set; in other words, whenever there is data in the Delta_X_L, Delta_XH, Delta_Y_L or Delta_Y_H registers. Clearing the motion bit (by reading Delta_X_L, Delta_XH, Delta_Y_L and Delta_Y_H, or writing to the Motion register) will put the motion pin high.

Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. This is true for all transactions including PROM download. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction. To improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because ESD and EFT/B events could be interpreted as serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.

Write Operation

Write operation, defined as data going from the micro-controller to the ADNS-9500 Sensor, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The ADNS-9500 Sensor reads MOSI on rising edges of SCLK.

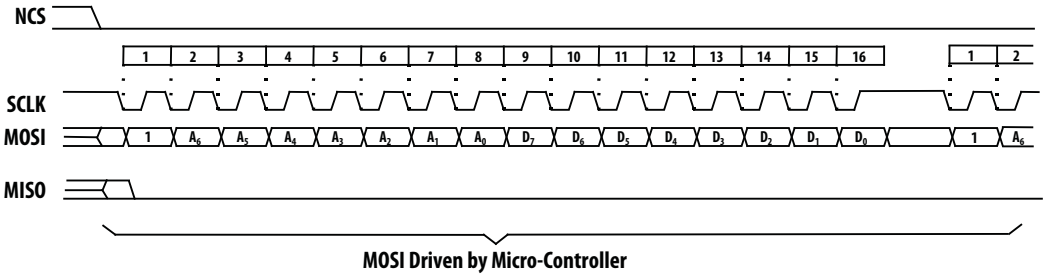


Figure 13. Write Operation

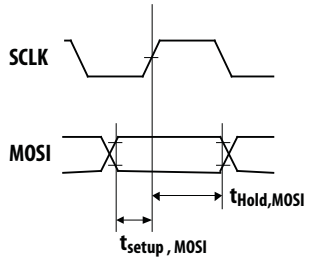


Figure 14. MOSI Setup and Hold Time

Read Operation

A read operation, defined as data going from the ADNS-9500 Sensor to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is sent by the micro-controller over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the ADNS-9500 Sensor over MISO. The sensor outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.

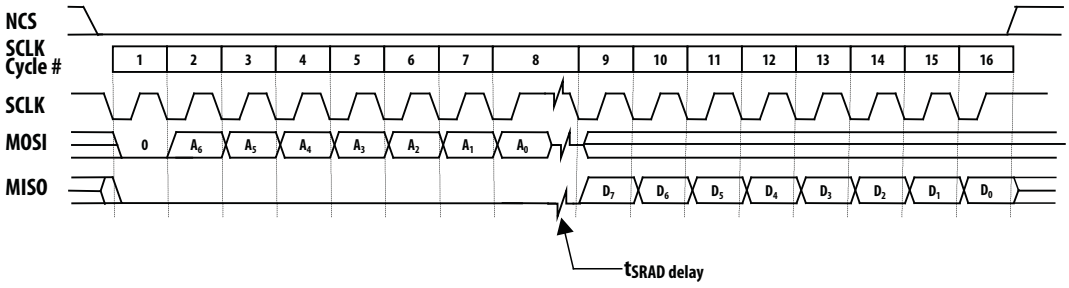


Figure 15. Read Operation

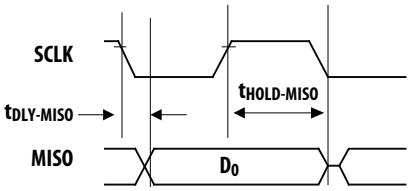


Figure 16. MISO Delay and Hold Time

NOTE:
The minimum high state of SCLK is also the minimum MISO data hold time of the ADNS-9500 Sensor. Since the falling edge of SCLK is actually the start of the next read or write command, the ADNS-9500 Sensor will hold the state of data on MISO until the falling edge of SCLK.

Required timing between Read and Write Commands (tsxx)

There are minimum timing requirements between read and write commands on the serial port.

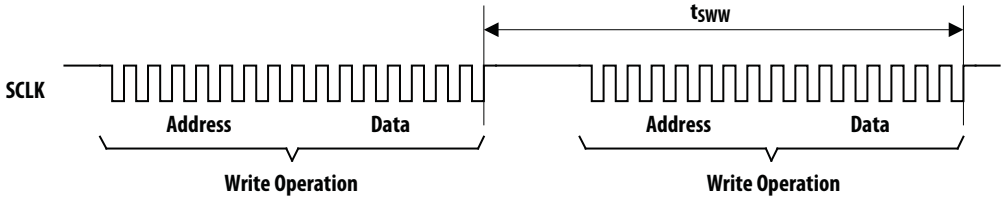


Figure 17. Timing between two write commands

If the rising edge of the SCLK for the last data bit of the second write command occurs before the tsww delay, then the first write command may not complete correctly.

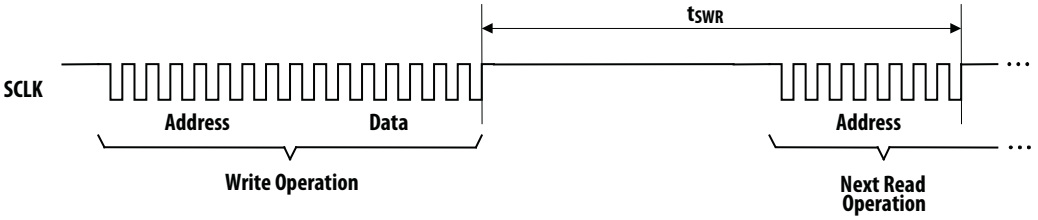


Figure 18. Timing between write and read commands

If the rising edge of SCLK for the last address bit of the read command occurs before the tswr required delay, the write command may not complete correctly.

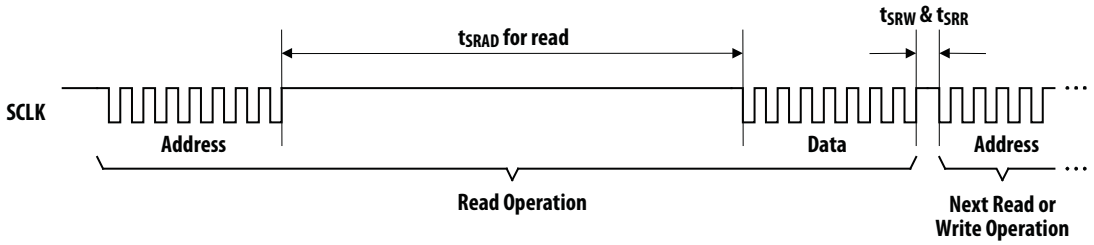


Figure 19. Timing between read and either write or subsequent read commands

During a read operation SCLK should be delayed at least tSRAD after the last address data bit to ensure that the Sensor has time to prepare the requested data.

The falling edge of SCLK for the first address bit of either the read or write command must be at least TSRR or TSRW after the last SCLK rising edge of the last data bit of the previous read operation. In addition, during a read operation SCLK should be delayed after the last address data bit to ensure that the ADNS-9500 Sensor has time to prepare the requested data.

Burst Mode Operation

Burst mode is a special serial port operation mode which may be used to reduce the serial transaction time for three predefined operations: motion read, PROM download and frame capture. The speed improvement is achieved by continuous data clocking to or from multiple registers without the need to specify the register address, and by not requiring the normal delay period between data bytes.

Motion Burst Read

Reading the Motion_Burst register activates this mode. The ADNS-9500 sensor will respond with the contents of the Motion, Observation, Delta_X_L, Delta_X_H, Delta_Y_L, Delta_Y_H, Pixel Statistic, Shutter and Frame period registers in that order. After sending the register address, the micro-controller must wait one frame, and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data are latched into the output buffer after the last address bit is received. After the burst transmission is complete, the micro-controller must raise the NCS line for at least tBEXIT to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

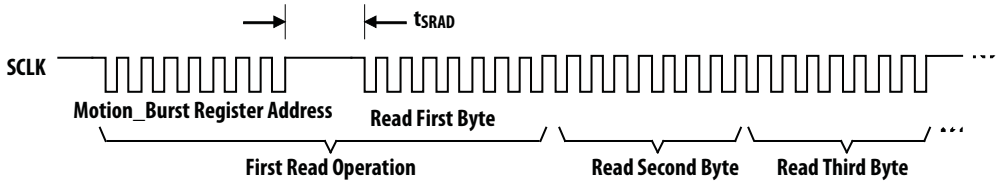


Figure 20. Motion Burst Timing

Procedure to start motion burst:

1. Lower NCS
2. Send 0x50 to Motion_Burst register.
3. Wait for one frame. (This only applicable in Run mode for wakeup but not require for rest mode)
4. Start reading SPI Data continuously up to 14bytes. Motion burst may be terminated by pulling NCS high for at least t_{BEXIT}.
5. To read new motion burst data, repeating from step 1.
6. Write any value to Motion register (address 0x02) to clear any residual motion.

Motion burst reporting:

BYTE [00] = Motion
BYTE [01] = Observation
BYTE [02] = Delta_X_L
BYTE [03] = Delta_X_H
BYTE [04] = Delta_Y_L
BYTE [05] = Delta_Y_H
BYTE [06] = SQUAL
BYTE [07] = Pixel_Sum
BYTE [08] = Maximum_Pixel
BYTE [09] = Minimum_Pixel
BYTE [10] = Shutter_Upper
BYTE [11] = Shutter_Lower
BYTE [12] = Frame_Period_Upper
BYTE [13] = Frame_Period_Lower

Note: In rest mode, motion burst data is always available or in other words, motion burst data can be read from Motion_Burst register even in rest modes.

SROM Download

This function is used to load the Avago supplied firmware file contents into the ADNS-9500 after sensor power up sequence. The firmware file is an ASCII text file. There are 2 methods of SROM downloading in ADNS-9500:1.5K and 3K bytes. 1.5K SROM download will only download 1.5K bytes data into the first half of SROM and leave the rest empty, while 3K SROM download will download the full 3K bytes data into SROM. They can be selected through Configuration_IV register, where default setting is 1.5K SROM download. In the current version of ADNS-9500 sensor, 3K bytes of SROM will be used.

SROM download procedure:

1. Select the 3K bytes SROM size at Configuration_IV register, address 0x39
2. Write 0x1d to SROM_Enable register for initializing
3. Wait for one frame
4. Write 0x18 to SROM_Enable register again to start SROM downloading
5. Write SROM file into SROM_Load_Burst register, 1st data must start with SROM_Load_Burst register address. All the SROM data must be downloaded before SROM start running.

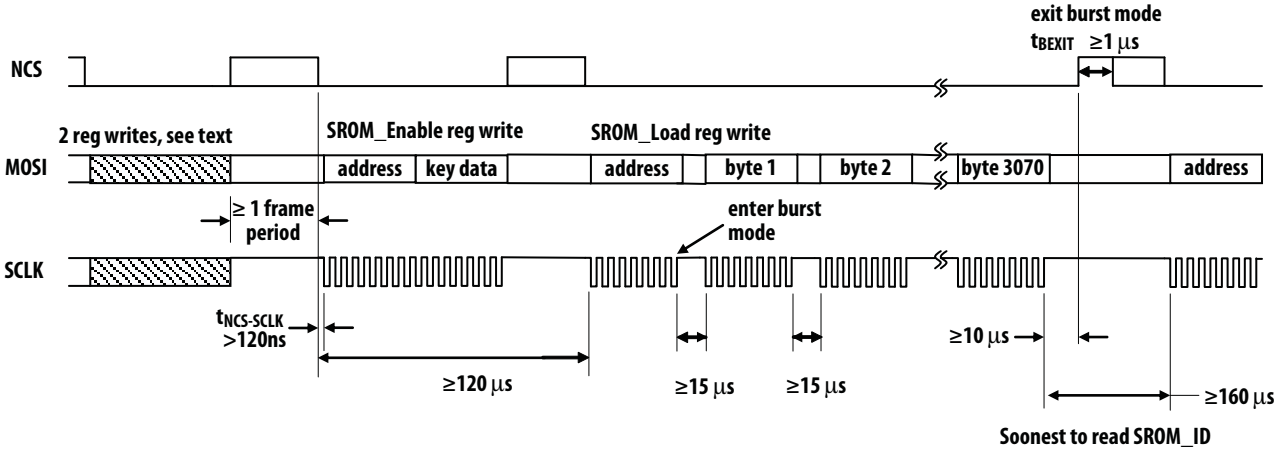


Figure 21. SROM Download Burst Mode

Frame Capture

This is a fast way to download a full array of pixel values from a single frame. This mode disables navigation and overwrites any downloaded firmware. A hardware reset is required to restore navigation, and the SROM firmware must be reloaded.

To trigger the capture, write to the Frame_Capture register. The next available complete 1 frame image will be stored to memory. The data are retrieved by reading the Pixel_Burst register once using the normal read method, after which the remaining bytes are clocked out by driving SCLK at the normal rate. If the Pixel_Burst register is read before the data is ready, it will return all zeros.

Procedure of Frame Capture:

1. Reset the chip by writing 0x5a to Power_Up_Reset register (address 0x3a).
2. Enable laser by setting Forced_Disable bit (bit-0) of LASER_CTRL0 register to 0.
3. Write 0x93 to Frame_Capture register.
4. Write 0xc5 to Frame_Capture register.
5. Wait for two frames.
6. Check for first pixel by reading bit zero of Motion register. If =1, first pixel is available.
7. Continue read from Pixel_Burst register until all 900 pixels are transferred.
8. Continue step 3-7 to capture another frame.

Note: Manual reset and SROM download are needed after frame capture to restore navigation for motion reading.

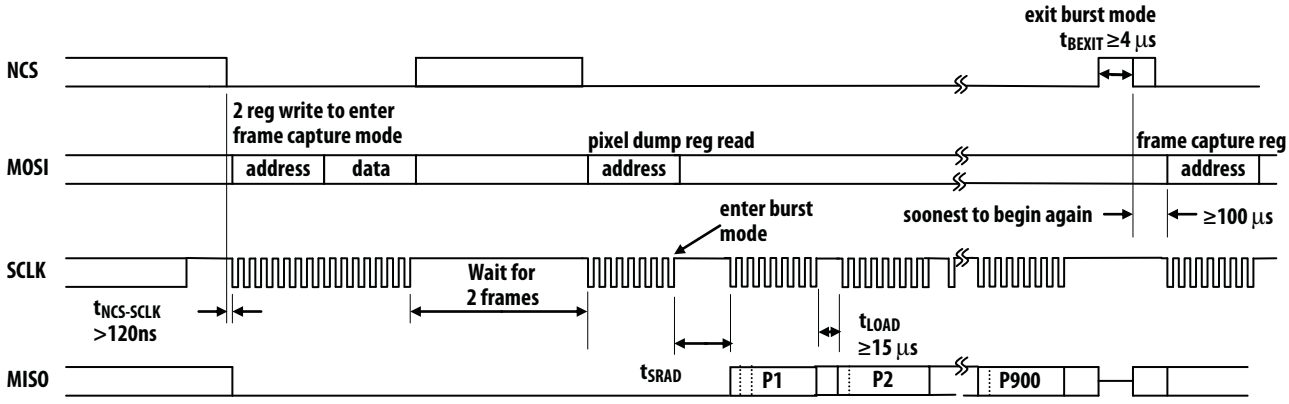


Figure 22. Frame Capture Burst Mode

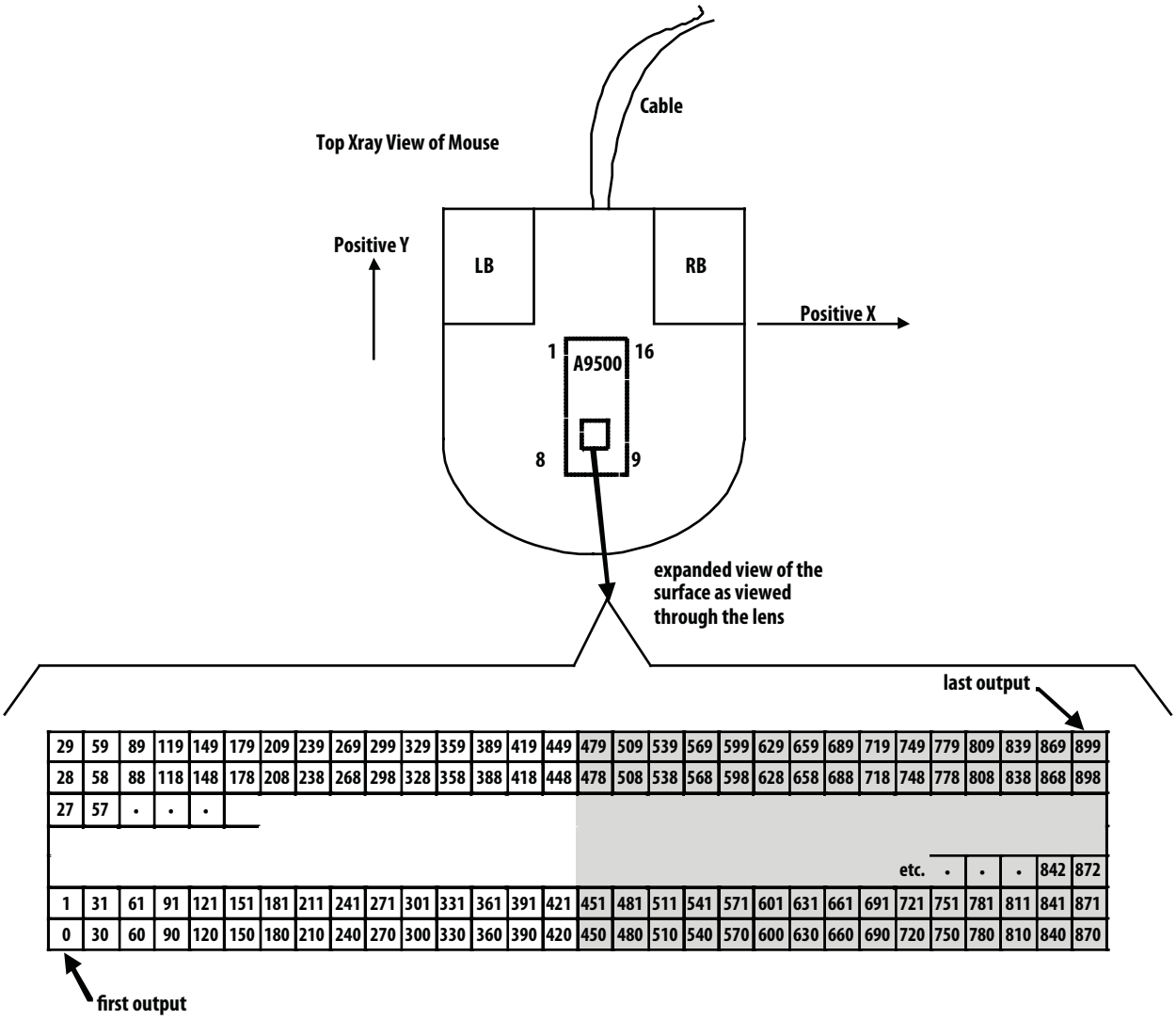


Figure 23. Pixel Map (Surface referenced)

Power Up

The ADNS-9500 Sensor does not perform an internal power up self-reset; the Power_Up_Reset register must be written every time power is applied. The appropriate sequence is as follows:

1. Apply power to VDD5/VDD3 and VDDIO in any order
2. Drive NCS high, and then low to reset the SPI port.
3. Write 0x5a to Power_Up_Reset register (address 0x3a).
4. Wait for at least 50ms time.
5. Read from registers 0x02, 0x03, 0x04, 0x05 and 0x06 (or read these same 5 bytes from burst motion register) one time regardless of the motion pin state.
6. SROM download.
7. Enable laser by setting Forced_Disable bit (bit-0) of LASER_CTRL0 register (address 0x20) to 0.

During power-up there will be a period of time after the power supply is high but before any clocks are available. The table below shows the state of the various pins during power-up and reset.

State of Signal Pins After VDD is Valid

Pin	On Power-Up	NCS High before Reset	NCS Low before Reset	After Reset
NCS	Functional	Hi	Low	Functional
MISO	Undefined	Undefined	Functional	Depends on NCS
SCLK	Ignored	Ignored	Functional	Depends on NCS
MOSI	Ignored	Ignored	Functional	Depends on NCS
MOTION	Undefined	Undefined	Undefined	Functional
LASER_NEN	Undefined	Undefined	Undefined	Functional

Shutdown

The ADNS-9500 can be set in Shutdown mode by writing 0xb6 to register 0x3b. The SPI port should not be accessed when Shutdown mode is asserted, except the power-up command (writing 0x5a to register 0x3a). (Other ICs on the same SPI bus can be accessed, as long as the sensor's NCS pin is not asserted.) The table below shows the state of various pins during shutdown. To deassert Shutdown mode:

1. Drive NCS high, then low to reset the SPI port.
2. Write 0x5a to Power_Up_Reset register (address 0x3a).
3. Wait for at least 50ms time.
4. Clear observation register.
5. Wait at least one frame and check observation register, Bit[5:0] must be set.
6. Read from registers 0x02, 0x03, 0x04, 0x05 and 0x06 (or read these same 5 bytes from burst motion register) one time regardless of the motion pin state.
7. SROM download.
8. Enable laser by setting Forced_Disable bit (bit-0) of LASER_CTRL0 register to 0.
9. Any register setting must then be reloaded.

Pin	Status when Shutdown Mode
NCS	Functional *1
MISO	Undefined *2
SCLK	Ignore if NCS = 1 *3
MOSI	Ignore if NCS = 1 *4
LASER_NEN	High (off)
MOTION	Undefined *2

*1 NCS pin must be held to 1 (high) if SPI bus is shared with other devices. It is recommended to hold to 1 (high) during Power Down unless powering up the Sensor. It must be held to 0 (low) if the sensor is to be re-powered up from shutdown (writing 0x5a to register 0x3a).

*2 Depends on last state. MISO should be configured to drive LOW during shutdown to meet the low current consumption as specified in the datasheet. This can be achieved by reading Inverse_Product_ID register (address 0x3f) since the return value (0xcc) on MISO line ends in a 0 (low state).

*3 SCLK is ignored, if NCS is 1 (high). It is functional if NCS is 0 (low).

*4 MOSI is ignored, if NCS is 1 (high). If NCS is 0 (low), any command present on the MOSI pin will be ignored except power-up command (writing 0x5a to register 0x3a).

Note:
There are long wakeup times from shutdown and forced Rest. These features should not be used for power management during normal mouse motion.

Registers

The ADNS-9500 registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Address	Register	Read/Write	Default Value
0x00	Product_ID	R	0x33
0x01	Revision_ID	R	0x03
0x02	Motion	R	0x00
0x03	Delta_X_L	R	0x00
0x04	Delta_X_H	R	0x00
0x05	Delta_Y_L	R	0x00
0x06	Delta_Y_H	R	0x00
0x07	SQUAL	R	0x00
0x08	Pixel_Sum	R	0x00
0x09	Maximum_Pixel	R	0x00
0x0a	Minimum_Pixel	R	0x00
0x0b	Shutter_Lower	R	0x20
0x0c	Shutter_Upper	R	0x4e
0x0d	Frame_Period_Lower	R	0xc0
0x0e	Frame_Period_Upper	R	0x5d
0x0f	Configuration_I	R/W	0x12
0x10	Configuration_II	R/W	0x00
0x12	Frame_Capture	R/W	0x00
0x13	SROM_Enable	W	0x00
0x14	Run_Downshift	R/W	0x32
0x15	Rest1_Rate	R/W	0x01
0x16	Rest1_Downshift	R/W	0x1f
0x17	Rest2_Rate	R/W	0x09
0x18	Rest2_Downshift	R/W	0xbc
0x19	Rest3_Rate	R/W	0x31
0x1a	Frame_Period_Max_Bound_Lower	R/W	0xc0
0x1b	Frame_Period_Max_Bound_Upper	R/W	0x5d
0x1c	Frame_Period_Min_Bound_Lower	R/W	0xa0
0x1d	Frame_Period_Min_Bound_Upper	R/W	0x0f
0x1e	Shutter_Max_Bound_Lower	R/W	0x20
0x1f	Shutter_Max_Bound_Upper	R/W	0x4e
0x20	LASER_CTRL0	R/W	0x01
0x21- 0x23	Reserved		
0x24	Observation	R/W	0x00
0x25	Data_Out_Lower	R	Undefined
0x26	Data_Out_Upper	R	Undefined
0x27 - 0x29	Reserved		
0x2a	SROM_ID	R	0x00
0x2e	Lift_Detection_Thr	R/W	0x10
0x2f	Configuration_V	R/W	0x12
0x30 - 0x38	Reserved		
0x39	Configuration_IV	R/W	0x00
0x3a	Power_Up_Reset	W	NA
0x3b	Shutdown	W	Undefined
0x3c - 0x3e	Reserved		
0x3f	Inverse_Product_ID	R	0xcc
0x40 – 0x4f	Reserved		
0x50	Motion_Burst	R	0x00
0x62	SROM_Load_Burst	W	Undefined
0x64	Pixel_Burst	R	0x00

Product_ID Address: 0x00
Access: Read Only Reset Value: 0x33

Bit	7	6	5	4	3	2	1	0
Field	PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Data Type: 8-bit unsigned integer.

USAGE: This value is a unique identification assigned to this model only. The value in this register does not change; it can be used to verify that the serial communications link is functional.

Revision_ID Address: 0x01
Access: Read Only Reset Value: 0x03

Bit	7	6	5	4	3	2	1	0
Field	RID_7	RID_6	RID_5	RID_4	RID_3	RID_2	RID_1	RID_0

Data Type: 8-bit unsigned integer.

USAGE: This register contains the current IC revision, the revision of the permanent internal firmware. It is subject to change when new IC versions are released.

Motion			Address: 0x02					
Access: Read Only			Reset Value: 0x00					
Bit	7	6	5	4	3	2	1	0
Field	MOT	FAULT	LP_Valid	Reserved	Reserved	OP_Mode_1	OP_Mode_2	FRAME_ Pix_First

Data Type: Bit field

USAGE: Register 0x02 allows the user to determine if motion has occurred since the last time it was read. If the MOT bit is set, Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H register should be read in sequence to get the accumulated motion. Read this register before reading the Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers as reading this register freezes the Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H register values. If Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers are not read before the Motion register is read for the second time, the data in Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H will be lost. Writing anything to this register clears the MOT bit, Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers. The written data byte is not saved.

It also tells if laser fault, laser power setting status and operating mode in current frame.

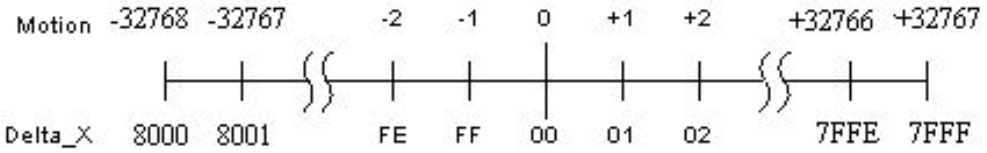
Field Name	Description
MOT	Motion since last report or Shutdown **0 = No motion** 1 = Motion occurred, data ready for reading in Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers
FAULT	Indicates that the XY_LASER is shorted to GND. **0 = no fault detected** 1 = fault detected
LP_Valid	Laser Power Settings **0 = Laser power register values do not have complementary values** 1 = laser power is valid
OP_Mode[1:0]	Operating mode of the sensor **00 = Run** 01 = Rest 1 10 = Rest 2 11 = Rest 3
FRAME_Pix_First	This bit is set to indicate first pixel in frame capture. **0 = Frame capture data not from pixel 0,0** 1 = Frame capture data is from pixel 0,0

Delta_X_L Address: 0x03
Access: Read Only Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0

Data Type: 16 bits 2's complement number. Lower 8 bits of Delta_X.

USAGE: X movement is counts since last report. Absolute value is determined by resolution. Reading it clears the register.



Delta_X_H Address: 0x04
Access: Read Only Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	X_8

Data Type: 16 bits 2's complement number. Upper 8 bits of Delta_X.

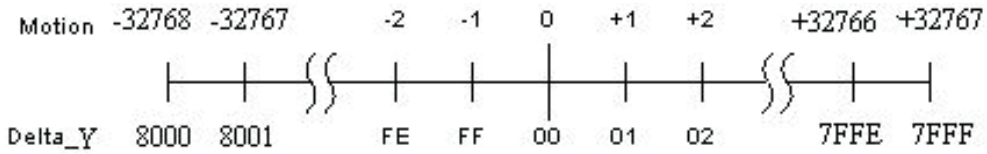
USAGE: Delta_X_H must be read after Delta_X_L to have the full motion data. Reading it clears the register.

Delta_Y_L Address: 0x05
Access: Read Only Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0

Data Type: 16 bits 2's complement number. Lower 8 bits of Delta_Y.

USAGE: Y movement is counts since last report. Absolute value is determined by resolution. Reading it clears the register.



Delta_Y_H Address: 0x06
Access: Read Only Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8

Data Type: 16 bits 2's complement number. Upper 8 bits of Delta_Y.

USAGE: Delta_Y_H must be read after Delta_Y_L to have the full motion data. Reading it clears the register.

NOTES: Avago RECOMMENDS that registers 0x02, 0x03, 0x04, 0x05 and 0x06 to be read sequentially.

SQUAL			Address: 0x07					
Access: Read Only			Reset Value: 0x00					
Bit	7	6	5	4	3	2	1	0
Field	SQ_7	SQ_6	SQ_5	SQ_4	SQ_3	SQ_2	SQ_1	SQ_0

Data Type: Upper 8-bits of a 10-bit unsigned integer.

USAGE: The SQUAL (Surface quality) register is a measure of the number of valid features visible by the sensor in the current frame. Use the following formula to find the total number of valid features.

Number of Features = SQUAL Register Value * 4

The maximum SQUAL register value is 169. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected. The graph below shows 800 sequentially acquired SQUAL values, while a sensor was moved slowly over white paper. SQUAL is nearly equal to zero if there is no surface below the sensor. SQUAL remains fairly high throughout the Z-height range which allows illumination of most pixels in the sensor.

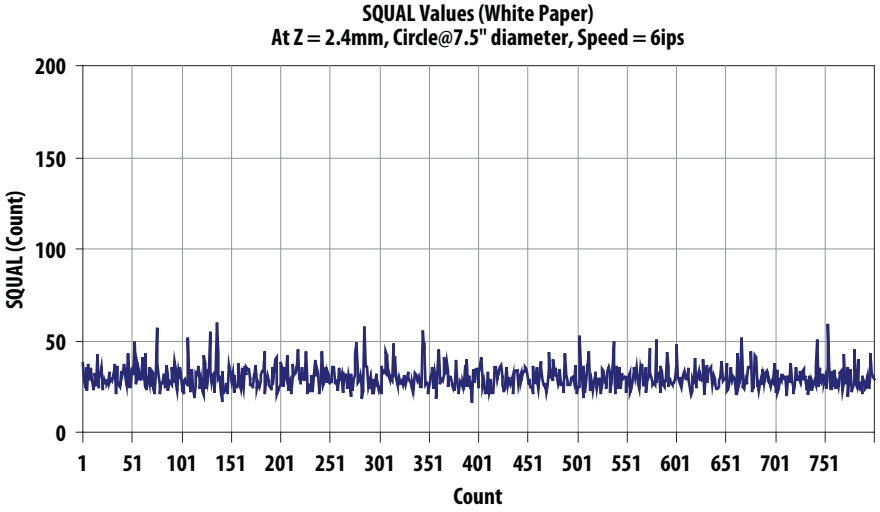


Figure 24. SQUAL Values at 1600cpi (White Paper)

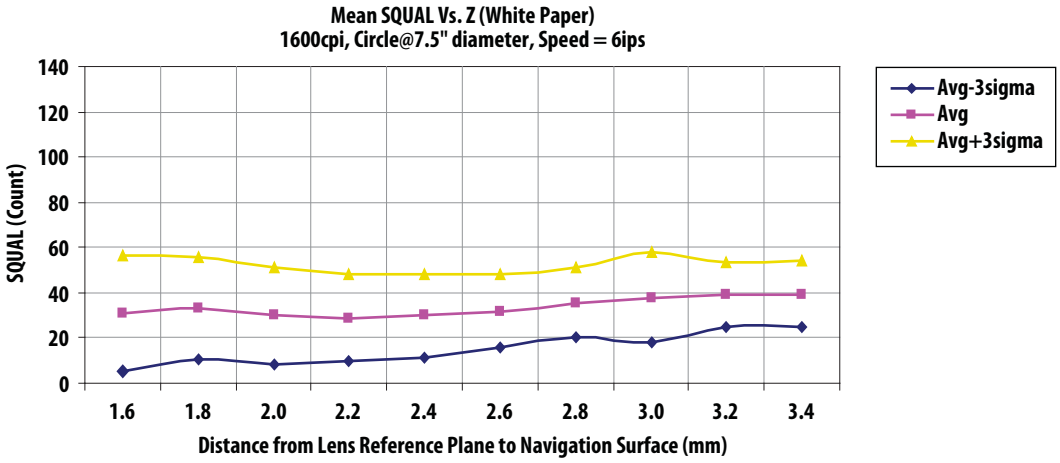


Figure 25. Mean SQUAL vs. Z (White Paper)

Pixel_Sum Address: 0x08
Access: Read Only Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	AP_7	AP_6	AP_5	AP_4	AP_3	AP_2	AP_1	AP_0

Data Type: High 8-bits of an unsigned 17-bit integer.

USAGE: This register is used to find the average pixel value. It reports the upper byte of a 17-bit counter which sums all 900 pixels in the current frame. It may be described as the full sum divided by 512. To find the average pixel value, follows the formula below.

Average Pixel = Register Value * 512/900 ≅ Register Value/1.76

The maximum register value is 223 (127 * 900/512 truncated to an integer). The minimum register value is 0. The pixel sum value can change every frame.

Maximum_Pixel Address: 0x09
Access: Read Only Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MP_7	MP_6	MP_5	MP_4	MP_3	MP_2	MP_1	MP_0

Data Type: Seven bit number.

USAGE: Maximum Pixel value in current frame. Minimum value = 0, maximum value = 127. The maximum pixel value can be adjusted every frame.

Minimum_Pixel Address: 0x0A
Access: Read Only Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	$MinP_7$	$MinP_6$	$MinP_5$	$MinP_4$	$MinP_3$	$MinP_2$	$MinP_1$	$MinP_0$

Data Type: Seven bit number.

USAGE: Minimum Pixel value in current frame. Minimum value = 0, maximum value = 127. The maximum pixel value can be adjusted every frame.

Shutter_Lower Address: 0x0B
Access: Read Only Reset Value: 0x20

Bit	7	6	5	4	3	2	1	0
Field	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

Shutter_Upper Access: Read Only			Address: 0x0C Reset Value: 0x4e					
Bit	7	6	5	4	3	2	1	0
Field	S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8

Data Type: 16-bit unsigned number.

USAGE: Units are clock cycles of internal oscillator (nominally 47MHz). Read Shutter_Upper first, then Shutter_Lower. They should be read consecutively. The shutter is adjusted to keep the average pixel values within normal operating ranges. The shutter value is checked and automatically adjusted to a new value if needed on every frame when operating in default mode. The shutter value can be set manually by disabling the AGC using the Configuration_II register and writing to the Shutter_Maximum_Bound registers. Because the automatic frame rate feature is related to shutter value it may also be appropriate to enable the fixed frame rate mode using the Configuration_II register. The maximum value of the shutter is dependent upon the setting in the Shutter_Maximum_Bound registers.

Shown below is a graph of 800 sequentially acquired shutter values, while the sensor was moved slowly over white paper.

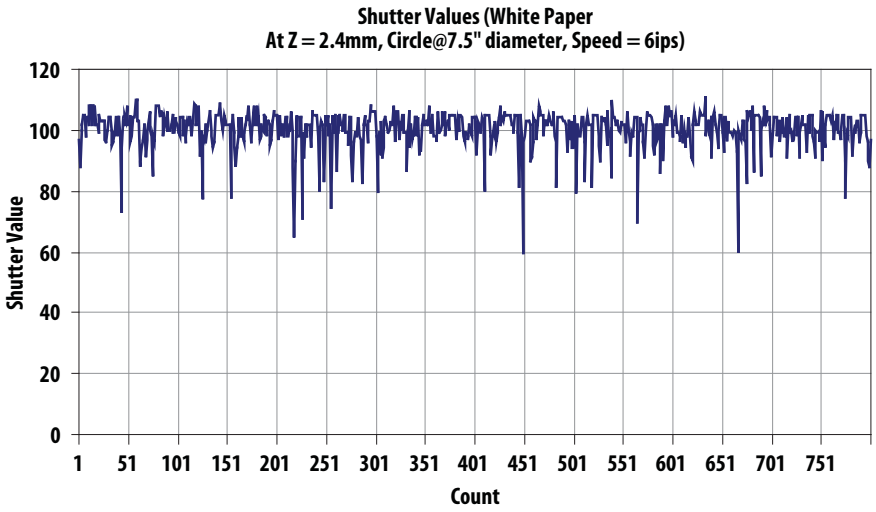


Figure 26. Shutter Values at 5000cpi (White Paper)

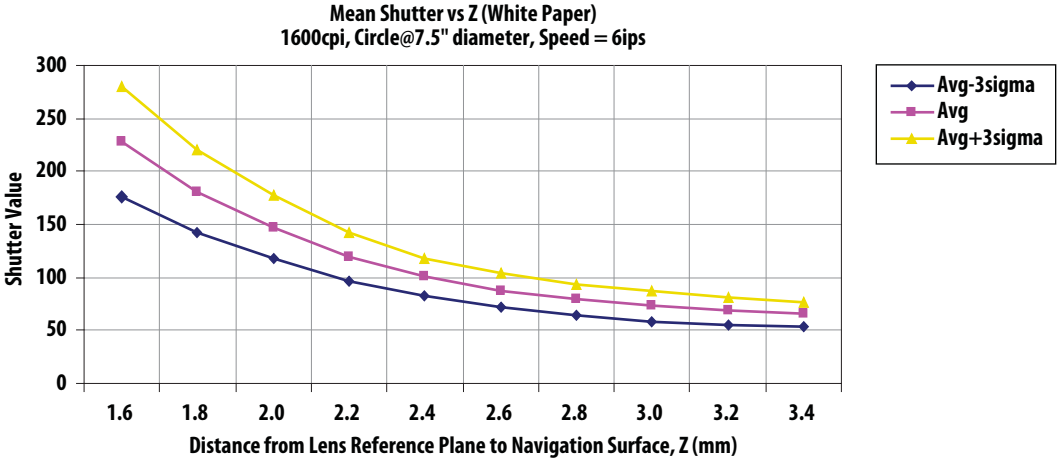


Figure 27. Mean Shutter vs. Z (White Paper)

Frame_Period_Lower Address: 0x0D
Access: Read Only Reset Value: 0xc0

Bit	7	6	5	4	3	2	1	0
Field	FP_7	FP_6	FP_5	FP_4	FP_3	FP_2	FP_1	FP_0

Frame_Period_Upper Address: 0x0E
Access: Read Only Reset Value: 0x5d

Bit	7	6	5	4	3	2	1	0
Field	FP_{15}	FP_{14}	FP_{13}	FP_{12}	FP_{11}	FP_{10}	FP_9	FP_8

Data Type: 16-bit unsigned integer.

USAGE: To read from the registers, read Frame_Period_Upper first followed by Frame_Period_Lower. If the Frame_Period_Upper register greater the zero, these registers provide the Run mode frame rate period. Read these registers to determine the run mode frame period, or indirectly the run mode frame rate. Units are clock cycles of the internal oscillator (nominally 47MHz). The formula is:

Run Mode's Frame Rate = Clock Frequency/Register Value

If the Frame_Period_Upper register is zero, these register provide the Rest mode frame rate period. Read these register to determine the rest mode frame period, or indirectly the rest mode frame rate. Units are clock cycles of the internal oscillator (nominally 100Hz). The formula is:

Rest Mode Frame Rate = 1 / [Register Value +1]

To set the frame rate manually, disable automatic frame rate mode via the Configuration_II register and write the desired count value to the Frame_Period_Maximum_Bound registers.

Configuration_I Address: 0x0F
Access: R/W Reset Value: 0x12

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	RES_5	RES_4	RES_3	RES_2	RES_1	RES_0

Data Type: Bit Field.

USAGE: This register sets the resolution on XY axes or X axis only. The approximate resolution value for each register setting can be calculated using the following formula. Each bit change is ~90cpi. The maximum write value is 0x38, which the resolution setting is approximately 5000cpi.

Resolution value (counts per inch, cpi) ≈ RES [5:0] x 90

For example:

Configuration_I Register Value	**Approximate Resolution (cpi)**	**Description**
0x01	90	Minimum
0x12	**1620**	**Default**
0x24	3240	
0x38	5040	Maximum

Note: Rpt_Mod bit in Configuration_II register is used to select CPI reporting mode either XY axes resolution setting in sync or independent setting for X-axis and Y-axis respectively. Refer to Configuration_V register for Y-axis resolution setting.

Configuration_II Address: 0x10
Access: R/W Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	F_Rest_1	F_Rest_0	Rest_En	NAGC	Fixed_FR	Rpt_Mod	0	0

Data Type: Bit Field.

USAGE: This register is used to change configuration of sensor.

When the sensor is put into Force Rest function via F_Rest[1:0], the operation mode of sensor will change from current mode to the next desired Rest mode and stay at the desired Rest mode until the Force Rest mode is released. Once Force Rest mode is released, the sensor will resume to normal operation from the desired Rest mode and auto downshift to the next level of Rest modes if no motion or recover to Run mode if motion is detected.

For example:

Current mode	**Next desired mode**	**Force Rest mode action**	**After Force Rest mode is released (F_Rest[1:0] = 00)**
Run	Rest1	Force Rest1 F_Rest[1:0] = 01	Resume to normal operation from REST1, auto downshift to Rest2, then Rest3 in sequence if no motion or back to Run mode if motion detected.
Run	Rest2	Force Rest2 F_Rest[1:0] = 10	Resume to normal operation from REST2, auto downshift to Rest3 if no motion or back to Run mode if motion detected.
Run	Rest3	Force Rest3 F_Rest[1:0] = 11	Resume to normal operation from REST3, stay in Rest3 if no motion or back to Run mode if motion detected.

Field Name	**Description**
F_Rest[1:0]	Puts chip into Rest mode **00 = Normal operation** 01 = Force Rest1 10 = Force Rest2 11 = Force Rest3
Rest_En	Enable Rest mode **0 = Normal operation without REST modes** 1 = REST modes enabled
NAGC	Disable AGC. Shutter value will be set to the value in the Shutter_Maximum_Bound registers. **0 = no, AGC is active** 1 = yes, AGC is disabled
Fixed_FR	Fixed frame rate (disable automatic frame rate control). When this bit is set the frame rate will be set by the value in the Frame_Period_Maximum_Bound registers. **0 = automatic frame rate** 1 = fixed frame rate
Rpt_Mod	Select CPI reporting mode. **0 = XY axes CPI setting in sync** 1 = CPI setting independently for X-axis and Y-axis. Configuration_I register sets X-axis resolution, while Configuration_V register sets Y-axis resolution.
Bit[1:0]	Must be set to 00

Frame_Capture Address: 0x12
Access: R/W Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	FC_7	FC_6	FC_5	FC_4	FC_3	FC_2	FC_1	FC_0

Data Type: Bit Field.

USAGE: Used to capture the next available complete 1 frame of pixel values to be stored to SROM RAM. Writing to this register will cause any firmware loaded in the SROM to be overwritten and stops navigation. A hardware reset and SROM download are required to restore normal operation for motion reading. Refer to Frame Capture section for use details.

SROM_Enable Address: 0x13
Access: Write Only Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	SE_7	SE_6	SE_5	SE_4	SE_3	SE_2	SE_1	SE_0

Data Type: 8 Bit number.

USAGE: Write to this register to start either SROM download or SROM CRC test. See SROM Download section for details SROM download procedure.

SROM CRC test can be performed to check for the successful of SROM downloading procedure. SROM CRC test is only valid after SROM downloaded. Navigation is halted and the SPI port should not be used during this SROM CRC test. Avago recommends reading the Motion register to determine the laser fault condition before performing the SROM CRC test.

SROM CRC test procedure is as below:

1. Write 0x15 to SROM_Enable register to start SROM CRC test.
2. Wait for at least 10ms.
3. Read the CRC value from Data_Lower and Data_Upper registers.

Run_Downshift Address: 0x14
Access: R/W Reset Value: 0x32

Bit	7	6	5	4	3	2	1	0
Field	RD_7	RD_6	RD_5	RD_4	RD_3	RD_2	RD_1	RD_0

Data Type: 8 Bit number.

USAGE: This register set the Run to Rest 1 downshift time. Default value is 500ms. Use the formula below for calculation.

Run Downshift time (ms) = RD[7:0] x 10
Default = 50 x 10 = 500ms

All the above values are calculated base on system clock, which expected to have 20% tolerance.

Rest1_Rate Address: 0x15
Access: R/W Reset Value: 0x01

Bit	7	6	5	4	3	2	1	0
Field	$R1R_7$	$R1R_6$	$R1R_5$	$R1R_4$	$R1R_3$	$R1R_2$	$R1R_1$	$R1R_0$

Data Type: 8 Bit number.

USAGE: This register set the Rest 1 frame rate. Default value is 20ms. Use the formula below for calculation.

Rest1 frame rate = (R1R[7:0] + 1) x 10ms.
Default = (1 + 1) x 10 = 20ms

All the above values are calculated base on 100Hz Hibernate clock, which expected to have 40% tolerance.

Rest1_Downshift Address: 0x16
Access: R/W Reset Value: 0x1f

Bit	7	6	5	4	3	2	1	0
Field	$R1D_7$	$R1D_6$	$R1D_5$	$R1D_4$	$R1D_3$	$R1D_2$	$R1D_1$	$R1D_0$

Data Type: 8 Bit number.

USAGE: This register set the Rest 1 to Rest 2 downshift time. Default value is 9920ms. Use the formula below for calculation.

Rest1 Downshift time = R1D[7:0] x 16 x Rest1_Rate.
Default = 31 x 16 x 20 = 9920ms

All the above values are calculated base on 100Hz Hibernate clock, which expected to have 40% tolerance.

Rest2_Rate Address: 0x17
Access: R/W Reset Value: 0x09

Bit	7	6	5	4	3	2	1	0
Field	$R2R_7$	$R2R_6$	$R2R_5$	$R2R_4$	$R2R_3$	$R2R_2$	$R2R_1$	$R2R_0$

Data Type: 8 Bit number.

USAGE: This register set the Rest 2 frame rate. Default value is 100ms. Use the formula below for calculation.

Rest2 frame rate = (R2R[7:0] + 1) x 10ms.
Default = (9 + 1) x 10 = 100ms

All the above values are calculated base on 100Hz Hibernate clock, which expected to have 40% tolerance.

Rest2_Downshift Address: 0x18
Access: R/W Reset Value: 0xbc

Bit	7	6	5	4	3	2	1	0
Field	$R2D_7$	$R2D_6$	$R2D_5$	$R2D_4$	$R2D_3$	$R2D_2$	$R2D_1$	$R2D_0$

Data Type: 8 Bit number.

USAGE: This register set the Rest 2 to Rest 3 downshift time. Default value is 10mins. Use the formula below for calculation.

Rest2 Downshift time = R2D[7:0] x 32 x Rest2_Rate.
Default = 188 x 32 x 100 = 601600ms = 10mins

All the above values are calculated base on 100Hz Hibernate clock, which expected to have 40% tolerance.

Rest3_Rate Address: 0x19
Access: R/W Reset Value: 0x31

Bit	7	6	5	4	3	2	1	0
Field	$R3R_7$	$R3R_6$	$R3R_5$	$R3R_4$	$R3R_3$	$R3R_2$	$R3R_1$	$R3R_0$

Data Type: 8 Bit number.

USAGE: This register set the Rest 3 frame rate. Default value is 500ms. Use the formula below for calculation.

Rest3 frame rate = (R3R[7:0] + 1) x 10ms.
Default = (49 + 1) x 10 = 500ms

All the above values are calculated base on 100Hz Hibernate clock, which expected to have 40% tolerance.

Frame_Period_Max_Bound_Lower			Address: 0x1A					
Access: R/W			Reset Value: 0xc0					
Bit	7	6	5	4	3	2	1	0
Field	FBM_7	FBM_6	FBM_5	FBM_4	FBM_3	FBM_2	FBM_1	FBM_0

Frame_Period_Max_Bound_Upper			Address: 0x1B					
Access: R/W			Reset Value: 0x5d					
Bit	7	6	5	4	3	2	1	0
Field	FBM_{15}	FBM_{14}	FBM_{13}	FBM_{12}	FBM_{11}	FBM_{10}	FBM_9	FBM_8

Data Type: 16-bit unsigned integer.

USAGE: This value sets the maximum frame period (the MINIMUM frame rate) which may be selected by the automatic frame rate control, or sets the actual frame period when operating in manual mode. To read from the registers, read Upper first followed by Lower. To write to the registers, write Lower first, followed by Upper. Units are clock cycles of the internal oscillator (nominally 47MHz). The formula is:

Frame Rate (Frames/second, fps) = Clock Frequency / Register Value

To set the frame rate manually, disable automatic frame rate mode via the Configuration_II register and write the desired count value to these registers. Writing to the Frame_Period_Max_Bound_Upper and Lower registers also activates any new values in the following registers:

- Frame_Period_Max_Bound_Upper and Lower
- Frame_Period_Min_Bound_Upper and Lower
- Shutter_Max_Bound_Upper and Lower

Any data written to these registers will be saved but will not take effect until the write to the Frame_Period_Max_Bound_Upper and Lower is complete. After writing to this register, two complete frame times are required to implement the new settings. Writing to any of the above registers before the implementation is complete may put the chip into an undefined state requiring a reset.

The three bound registers must also follow this rule when set to non-default values. There is no protection against illegal register settings, which can impact the navigation.

Frame_Period_Max_Bound ≥ Frame_Period_Min_Bound + Shutter_Max_Bound.

The following table lists some Frame Period example values with a 47MHz clock.

	Frame Period		**Frame_Period Register Value**	
Frame Rate	**Decimal**	**Hex**	**Upper**	**Lower**
1,880	25,000	61a8	61	a8
1,958	**24,000**	**5dc0**	**5d**	**c0**
7,200	6,528	1980	19	80
11,750	4,000	0fa0	0f	a0

Frame_Period_Min_Bound_Lower Address: 0x1C
Access: R/W Reset Value: 0xa0

Bit	7	6	5	4	3	2	1	0
Field	FBm_7	FBm_6	FBm_5	FBm_4	FBm_3	FBm_2	FBm_1	FBm_0

Frame_Period_Min_Bound_Upper Address: 0x1D
Access: R/W Reset Value: 0x0f

Bit	7	6	5	4	3	2	1	0
Field	FBm_{15}	FBm_{14}	FBm_{13}	FBm_{12}	FBm_{11}	FBm_{10}	FBm_9	FBm_8

Data Type: 16-bit unsigned integer.

USAGE: This value sets the minimum frame period (the MAXIMUM frame rate) which may be selected by the automatic frame rate control. Units are clock cycles of the internal oscillator (nominally 47MHz). The minimum allowed write value is 0fa0, the maximum is 61a8. The Frame Rate formula is

Frame Rate (Frames/second, fps) = Clock Rate / Register Value

To read from the registers, read Upper first followed by Lower. To write to the registers, write Lower first, followed by Upper, then write anything to the Frame_Period_Max_Bound Lower and Upper registers to activate the new setting. A good practice is to read the content of the Frame_Period_Max_Bound registers and write it back.

Reading this register will return the most recent value that was written to it. However, the value will take effect only after a write to the Frame_Period_Max_Bound_Upper and Lower registers. After writing to Frame_Period_Max_Bound_Upper, wait at least two frame times before writing to Frame_Period_Min_Bound_Upper or Lower again. Refer to Frame_Period_Max_Bound register USAGE for details.

In addition, the three bound registers must also follow this rule when set to non-default values:

Frame_Period_Max_Bound ≥ Frame_Period_Min_Bound + Shutter_Max_Bound.

Shutter_Max_Bound_Lower Access: R/W			Address: 0x1E Reset Value: 0x20					
Bit	7	6	5	4	3	2	1	0
Field	SB_7	SB_6	SB_5	SB_4	SB_3	SB_2	SB_1	SB_0

Shutter_Max_Bound_Upper Access: R/W			Address: 0x1F Reset Value: 0x4e					
Bit	7	6	5	4	3	2	1	0
Field	SB_{15}	SB_{14}	SB_{13}	SB_{12}	SB_{11}	SB_{10}	SB_9	SB_8

Data Type: 16-bit unsigned integer.

USAGE: This value sets the maximum allowable shutter value when operating in automatic mode. Units are clock cycles of the internal oscillator (nominally 47MHz). Since the automatic frame rate function is based on shutter value, the value in these registers can limit the range of the frame rate control.

To read from the registers, read Upper first followed by Lower. To write to the registers, write Lower first, followed by Upper, then execute a write to the Frame_Period_Max_Bound_Upper and Lower registers to activate the new setting. A good practice is to read the content of the Frame_Period_Max_Bound registers and write it back. To set the shutter manually, disable the AGC via the Configuration_I register and write the desired value to these registers.

Reading this register will return the most recent value that was written to it. However, the value will take effect only after a write to the Frame_Period_Max_Bound_Upper and Lower registers. After writing to Frame_Period_Max_Bound_Upper, wait at least two frame times before writing to Shutter_Max_Bound_Upper or Lower again.

In addition, the three bound registers must also follow this rule when set to non-default values:

Frame_Period_Max_Bound ≥ Frame_Period_Min_Bound + Shutter_Max_Bound.

LASER_CTRL0 Address: 0x20
Access: R/W Reset Value: 0x01

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	CW_2	CW_1	CW_0	Force_ Disabled

Data Type: Bit field

USAGE: This register is used to control the laser drive mode.

Field Name	**Description**
CW[2:0]	Laser drive mode - Write 010b to bits [3,2,1] to set the laser to continuous ON (CW) mode. - Write 000b to exit laser continuous ON mode, all other values are not recommended. Reading the Motion register (0x02) will reset the value to 000b and exit laser continuous ON mode.
Force_Disabled	LASER force disabled 0 = LASER_NEN normal **1 = LASER_NEN force disabled**

Observation Address: 0x24
Access: R/W Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	OB_7	OB_6	OB_5	OB_4	OB_3	OB_2	OB_1	OB_0

Data Type: Bit field

USAGE: The user must clear the register by writing 0x00, wait for one frame, and read the register. The active processes will have set their corresponding bit. This register may be used as part of a recovery scheme to detect a problem caused by EFT/B or ESD.

Field Name	**Description**
OB_6	0 = chip is not running SROM code **1 = chip is running SROM code**
OB[5:0]	Set once per frame

Data_Out_Lower Address: 0x25
Access: Read Only Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	DO_7	DO_6	DO_5	DO_4	DO_3	DO_2	DO_1	DO_0

Data_Out_Upper Address: 0x26
Access: Read Only Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	DO_{15}	DO_{14}	DO_{13}	DO_{12}	DO_{11}	DO_{10}	DO_9	DO_8

Data Type: 16-bit word.

USAGE: Data in these registers come from the SROM CRC test. The data can be read out in either order. The SROM CRC test is initiated by writing 0x15 to SROM_Enable register.

CRC Result	Data_Out_Upper	Data_Out_Lower
SROM CRC test	BE	EF

SROM_ID Address: 0x2A
Access: Read Only Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	SR_7	SR_6	SR_5	SR_4	SR_3	SR_2	SR_1	SR_0

Data Type: 8-bit unsigned integer.

USAGE: Contains the revision of the downloaded Shadow ROM (SROM) firmware. If the firmware has been successfully downloaded and the chip is operating out of SROM, this register will contain the SROM firmware revision; otherwise it will contain 0x00.

Lift_Detection_Thr Address: 0x2E
Access: R/W Reset Value: 0x10

Bit	7	6	5	4	3	2	1	0
Field	Reserve	Reserve	Reserve	LD_Thr_4	LD_Thr_3	LD_Thr_2	LD_Thr_1	LD_Thr_0

Data Type: 8-bit unsigned integer.

USAGE: To configure the lift detection from the nominal Z-height of 2.4mm of navigation system when ADNS-9500 sensor is coupled with ADNS-6190-002 lens. Higher value will result in higher lift detection. Different surfaces will have different lift detection values with same setting due to different surface characteristic.

Configuration_V Address: 0x2F
Access: R/W Reset Value: 0x12

Bit	7	6	5	4	3	2	1	0
Field	$ResY_7$	$ResY_6$	$ResY_5$	$ResY_4$	$ResY_3$	$ResY_2$	$ResY_1$	$ResY_0$

Data Type: Bit field.

USAGE: This register allows the user to change the Y-axis resolution when the sensor is configured to have indepedent X-axis and Y-axis resolution reporting mode via Rpt_Mod bit = 1 in Configuration_II register. The setting in this register will be inactive if Rpt_Mod bit = 0. The approximate resolution value for each register setting can be calculated using the following formula. Each bit change is~90cpi. The minimum write value is 0x01 and maximum is 0x37.

Resolution value (counts per inch, cpi) = RES [7:0] x 90

Configuration_IV Address: 0x39
Access: R/W Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SROM_Size	Reserved

Data Type: Bit field.

USAGE: The correct SROM file size must be selected before loading the SROM to sensor. The current SROM is 3K Bytes size.

Field Name	Description
SROM_Size	**= 0: 1.5K SROM download** = 1: 3K SROM download

Power_Up_Reset Address: 0x3A
Access: Write Only Reset Value: 0xNA

Bit	7	6	5	4	3	2	1	0
Field	PUR_7	PUR_6	PUR_5	PUR_4	PUR_3	PUR_2	PUR_1	PUR_0

Data Type: 8-Bit integer.

USAGE: Write 0x5a to this register to reset the chip. All settings will revert to default values. Reset is required after recovering from shutdown mode and restore normal operation after Frame Capture.

Shutdown Address: 0x3B
Access: Write Only Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	OB_7	OB_6	OB_5	OB_4	OB_3	OB_2	OB_1	OB_0

Data Type: 8-Bit integer.

USAGE: Write 0xb6 to set the chip to shutdown mode, use POWER_UP_RESET register to power up the chip. Refer to Shutdown section for more details.

Inverse_Product_ID
Access: Read Only

Address: 0x3F
Reset Value: 0xcc

Bit	7	6	5	4	3	2	1	0
Field	PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Data Type: 8-Bit unsigned integer.

USAGE: This value is the inverse of the Product_ID, located at the inverse address. It is used to test the SPI port hardware.

Motion_Burst
Access: Read Only

Address: 0x50
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MB_7	MB_6	MB_5	MB_4	MB_3	MB_2	MB_1	MB_0

Data Type: 8-Bit unsigned integer.

USAGE: The Motion_Burst register is used for high-speed access to the Motion, Observation, Delta_X_L, Delta_X_H, Delta_Y_L, Delta_Y_H, SQUAL, Pixel_Sum, Maximum_Pixel, Minimum_Pixel, Shutter_Upper, Shutter_Lower, Frame_Period_Upper and Frame_Period_Lower registers. See Burst Mode-Motion Read section for use details. Write any value to this register will clear all motion burst data.

SROM_Load_Burst
Access: Write Only

Address: 0x62
Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	SL_7	SL_6	SL_5	SL_4	SL_3	SL_2	SL_1	SL_0

USAGE: The SROM_Load_Burst register is used for high-speed programming SROM from an external PROM or micro-controller. See SROM Download section for use details.

Pixel_Burst
Access: Read Only

Address: 0x64
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	PB_7	PB_6	PB_5	PB_4	PB_3	PB_2	PB_1	PB_0

Data Type: 8-Bit unsigned integer.

USAGE: The Pixel_Burst register is used for high-speed access to all the pixel values for one complete frame capture, without writing to the register address to obtain each pixel data. The data pointer is automatically incremented after each read so all 900 pixel values may be obtained by reading this register 900 times. See Frame Capture section for use details.

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